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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/460,742	12/14/1999	RAJENDRAN NAIR	884.229US1	2896
21186 . 759	21186 · 7590 10/17/2003		EXAMINER	
SCHWEGMAN, LUNDBERG, WOESSNER & KLUTH, P.A.			TRA, ANH QUAN	
	P.O. BOX 2938 MINNEAPOLIS, MN 55402			PAPER NUMBER
	•		2816	
			DATE MAILED: 10/17/2003	

Please find below and/or attached an Office communication concerning this application or proceeding.

		*				
	Application N .	Applicant(s)				
	09/460,742	NAIR ET AL.				
Office Action Summary	Examiner	Art Unit				
	Quan Tra	2816				
The MAILING DATE of this communication appears n the cover sheet with the correspondence address Period for Reply						
A SHORTENED STATUTORY PERIOD FOR REPLY THE MAILING DATE OF THIS COMMUNICATION. - Extensions of time may be available under the provisions of 37 CFR 1.13 after SIX (6) MONTHS from the mailing date of this communication. - If the period for reply specified above is less than thirty (30) days, a reply If NO period for reply is specified above, the maximum statutory period w - Failure to reply within the set or extended period for reply will, by statute, - Any reply received by the Office later than three months after the mailing earned patent term adjustment. See 37 CFR 1.704(b). Status	36(a). In no event, however, may a reply be time within the statutory minimum of thirty (30) day fill apply and will expire SIX (6) MONTHS from cause the application to become ABANDONE	nely filed s will be considered timely. the mailing date of this communication. D (35 U.S.C. § 133).				
1) Responsive to communication(s) filed on <u>18 A</u>	<u>ugust 2003</u> .					
2a) ☐ This action is FINAL . 2b) ☑ Thi	is action is non-final.					
 Since this application is in condition for allowal closed in accordance with the practice under Indicated the properties. Disposition of Claims 						
4) Claim(s) 4-6,9,10,14-16 and 29-37 is/are pend	ling in the application.					
4a) Of the above claim(s) is/are withdrawn from consideration.						
5) Claim(s) is/are allowed.						
6)⊠ Claim(s) <u>4-6,9,10,14-16 and 29-37</u> is/are rejected.						
7) Claim(s) is/are objected to.						
8) Claim(s) are subject to restriction and/or Application Papers	election requirement.					
9) The specification is objected to by the Examiner	•					
10)☐ The drawing(s) filed on is/are: a)☐ accepted or b)☐ objected to by the Examiner.						
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).						
11) The proposed drawing correction filed on is: a) approved b) disapproved by the Examiner.						
If approved, corrected drawings are required in reply to this Office action.						
12) The oath or declaration is objected to by the Examiner.						
Priority under 35 U.S.C. §§ 119 and 120						
13) Acknowledgment is made of a claim for foreign	priority under 35 U.S.C. § 119(a)-(d) or (f).				
a) ☐ All b) ☐ Some * c) ☐ None of:						
1. Certified copies of the priority documents have been received.						
2. Certified copies of the priority documents have been received in Application No						
 3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)). * See the attached detailed Office action for a list of the certified copies not received. 						
14) Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).						
a) The translation of the foreign language pro-	visional application has been rec	eived.				
Attachment(s)	5 p. 15 kg and 00 0.0.0. 33 120	GIGIOTET.				
Notice of References Cited (PTO-892) Notice of Draftsperson's Patent Drawing Review (PTO-948) Information Disclosure Statement(s) (PTO-1449) Paper No(s)	5) Notice of Informal F	(PTO-413) Paper No(s) Patent Application (PTO-152)				

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 08/18/2003 has been entered. A new ground of rejection is introduced as necessitated by amendment.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless -

- (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
- 3. Claims 9 and 10 rejected under 35 U.S.C. 102(b) as being anticipated by Mead et al. (USP 5844265).

As to claim 9, Mead et al discloses in figure 1 a circuit comprising a die having a high power supply voltage node (18) and low power supply voltage node (28); and a transistor (32) coupled between the high power supply voltage node and the low power supply voltage node and operable for controlling a voltage at the low power supply voltage node.

As to claim 10, figure 1 shows the transistor has a gate, a drain, and a source, and the gate is coupled to the high power supply voltage node and the source and drain are coupled to the low power supply voltage node.

Claim Rejections - 35 USC § 103

- 4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:
 - (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.
- 5. Claims 4-6, 14-16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Choi (USP 6060930) in view of Manning et al. (USP 5962887).

As to claim 4, Choi's figure 1 shows a circuit comprising: a voltage node (node between PM1 and NM1); a ground node (VSS); and a transistor (NM1') including a gate, drain and source, the gate being coupled to the voltage node and the drain and source being coupled to the ground node. Thus, figure 1 shows all limitations of the claim except for the detail of the capacitor connected transistor (NM1'). However, Manning et al.'s figure 1 shows a capacitor connected transistor including gate comprising p-type polysilicon (column 1, lines 52-58); a gate oxide layer (capacitor figure 1 is metal-oxide-semiconductor. Therefore, the dielectric layer 110 is oxide layer), a drain (130 or 140), and a source (140 or 130), the transistor to operate in the depletion mode (depending on the value of voltage 160, figure 2 shows transistor 2 is operating in depletion mode for certain of range). The capacitor connected transistor of Manning et al. has the advantage of increasing voltage range. Therefore, it would have been obvious to one having

ordinary skill in the art to use Manning et al.'s capacitor connected transistor for Choi's capacitor connected transistor (NM1') for the purpose of increasing the voltage range. Thus, the modified Choi's figure 1 shows all limitations of the claim except for the gate oxide layer having thickness of between 20 angstroms and about 40 angstroms. However, it is seen as an obvious matter of preference bounded by well known manufacturing constraints and ascertainable by routine experimentation and optimization to choose the particular claimed relative thickness limitations because applicant has not disclosed that the limitations are for a particular unobvious purpose, produce an unexpected result, or are otherwise critical, and it appears prima facie that the process would possess utility using another relative thickness. Indeed, it has been held that optimization of range limitations are prima facie obvious absent a disclosure that the limitations are for a particular unobvious purpose, produce an unexpected result, or are otherwise critical. See MPEP 2144.05(II): "Generally, differences in concentration or temperature will not support the patentability of subject matter encompassed by the prior art unless there is evidence indicating such concentration or temperature is critical. '[W]here the general conditions of a claim are disclosed in the prior art, it is not inventive to discover the optimum or workable ranges by routine experimentation." In re Aller, 220 F.2d 454, 105 USPO 233, 235 (CCPA 1955). See also In re Hoeschele, 406 F.2d 1403, 160 USPQ 809 (CCPA 1969), Merck & Co. Inc. v. Biocraft Laboratories Inc., 874 F.2d 804, 10 USPQ2d 1843 (Fed. Cir.), cert. denied, 493 U.S. 975 (1989), and In re Kulling, 897 F.2d 1147, 14 USPQ2d 1056 (Fed. Cir. 1990). As set forth in MPEP 2144.05(III), "Applicant can rebut a prima facie case of obviousness based on overlapping ranges by showing the criticality of the claimed range. 'The law is replete with cases in which the difference between the claimed invention and the prior art is some range or other variable

within the claims. . . . In such a situation, the applicant must show that the particular range is critical, generally by showing that the claimed range achieves unexpected results relative to the prior art range.' In re Woodruff, 919 F.2d 1575, 16 USPQ2d 1934 (Fed. Cir. 1990). See MPEP § 716.02 - § 716.02(g) for a discussion of criticality and unexpected results." Therefore, it would have been obvious to one having ordinary skill in the art to select the thickness of Manning et al.'s layer 110 to be between 20 angstroms and about 40 angstroms dependent upon particular environment of use to ensure optimum performance.

As to claim 14, the modified Choi's figure 1 shows a circuit comprising a die (circuit figure 1 is integrated circuit); a ground node (VSS) located on the die; power supply voltage node (node between PM1 and NM1); and an electronic device (the modified NM1') having a variable capacitance characteristic (Manning et al.'s figure 2) and that is permanently coupled between the ground node and the power supply voltage node and capable of providing a removal of charge at a constant rate for an asymmetrical to incremental voltage variations about an operational node voltage at the power supply voltage node (the modified Manning's transistor having similar structure with Applicant's transistor. Therefore, Manning et al.'s transistor is capable of perform similar function as Applicant's transistor).

As to claim 15, since electric property of the capacitor as shown in the modified Choi's figure 1 is the same as the claimed capacitor transistor whose property is shown in figure 1B of the application and the prior art discloses all the claimed structure, the accompanying characteristics including the damping and amplifying are inherent.

As to claims 5 and 16, Choi teaches that Vcc can be decreased (column 1, line 41), thereby decreasing voltage at node between PM1 and NM1. Thus, the modified Choi's figure 1

shows all limitations of the claim except for the voltage of at the node between PM1 and NM1 is between about 0.5 volts and about 1.5 volts or at 1.3 volts. However, it is seen as an obvious matter of preference bounded by well known manufacturing constraints and ascertainable by routine experimentation and optimization to choose the particular claimed relative operating voltage limitations because applicant has not disclosed that the limitations are for a particular unobvious purpose, produce an unexpected result, or are otherwise critical, and it appears prima facie that the process would possess utility using another relative operating voltage. Indeed, it has been held that optimization of range limitations are prima facie obvious absent a disclosure that the limitations are for a particular unobvious purpose, produce an unexpected result, or are otherwise critical. See MPEP 2144.05(II): "Generally, differences in concentration or temperature will not support the patentability of subject matter encompassed by the prior art unless there is evidence indicating such concentration or temperature is critical. '[W]here the general conditions of a claim are disclosed in the prior art, it is not inventive to discover the optimum or workable ranges by routine experimentation." In re Aller, 220 F.2d 454, 105 USPQ 233, 235 (CCPA 1955). See also In re Hoeschele, 406 F.2d 1403, 160 USPO 809 (CCPA 1969). Merck & Co. Inc. v. Biocraft Laboratories Inc., 874 F.2d 804, 10 USPO2d 1843 (Fed. Cir.), cert. denied, 493 U.S. 975 (1989), and In re Kulling, 897 F.2d 1147, 14 USPO2d 1056 (Fed. Cir. 1990). As set forth in MPEP 2144.05(III), "Applicant can rebut a prima facie case of obviousness based on overlapping ranges by showing the criticality of the claimed range. 'The law is replete with cases in which the difference between the claimed invention and the prior art is some range or other variable within the claims. . . . In such a situation, the applicant must show that the particular range is critical, generally by showing that the claimed range achieves

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unexpected results relative to the prior art range.' In re Woodruff, 919 F.2d 1575, 16 USPQ2d 1934 (Fed. Cir. 1990). See MPEP § 716.02 - § 716.02(g) for a discussion of criticality and unexpected results." Therefore, it would have been obvious to one having ordinary skill in the art to select the operating voltage for Choi's capacitor to be between about 0.5 volts and about 1.5 volts or at 1.3 volts (by selecting certain value of Vcc) dependent upon particular environment of use to ensure optimum performance.

As to claim 6, the modified Choi's figure 1 further shows a logic cell (IN1) coupled to the voltage node and close to the transistor.

6. Claim 29 is rejected under 35 U.S.C. 103(a) as being unpatentable over Choi (USP 6060930) in view of Manning et al. (USP 5962887) and Yoneda et al. (USP 4906594).

The combination of Choi and Manning et al. references (see the rejection of claim 4) teaches all elements of the claim except for the transistor formed on a silicon-on-sapphire (SOS) substrate. However, Yoneda et al. teaches in column 1, lines 35-40, that SOS substrate has excellent characteristics such as higher speed owing to decreased floating capacity. Thereby improving the operation characteristics for the integrated circuit. Therefore, it would have been obvious to one having ordinary skill in the art to use silicon-on-sapphire as a substrate of Choi's transistor for the purpose of improving the operation characteristic for the transistor.

7. Claims 30 ad 31 are rejected under 35 U.S.C. 103(a) as being unpatentable over Choi (USP 6060930) in view of Manning et al. (USP 5962887) and Yoneda et al. (USP 4906594) and Jones et al. (USP 5632855).

As to claim 30, the combination of Choi, Manning et al. Yoneda et al. references shows all limitations of the claim except for the oxide layer comprises a thermal oxide. However, Jones

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et al. teaches in column 1, lines 10-13, that thermal oxidation is the most viable way to form an oxide. Thermal oxide serves numerous purposes, such as preventing formation of certain types of thin films upon the oxide while allowing those types of films to form in area void of oxide. Thus, it would have been obvious to one having ordinary skill in the art to form the oxide layer by thermal oxidation process for the purpose of preventing formation of certain types of thin films upon the oxide while allowing those types of films to form in area void of oxide.

As to claim 31, the modified Choi's figure 1 further shows a logic cell (IN1) coupled to the voltage node and close to the transistor.

8. Claims 32-33 are rejected under 35 U.S.C. 103(a) as being unpatentable over Mead et al. (USP 5844265) in view of Abrokwah et al. (USP 5539248).

As to claim 32, Mead et al discloses in figure 1 a circuit comprising a die having a high power supply voltage node (18) and low power supply voltage node (28); and a transistor (32) coupled between the high power supply voltage node and the low power supply voltage node and operable for controlling a voltage at the low power supply voltage node. Thus, figure 1 shows all limitations of the claim except for gallium arsenide die. However, Abrokwah et al. teaches column 1, lines 15-16, that gallium arsenide devices have an advantage over silicon device in speed and power consumption. Therefore, it would have been obvious to one having ordinary skill in the art to use gallium arsenide as the substrate for Mead et al. circuit for the purpose of improving speed and power consumption.

As to claim 33, Mead et al.'s figure 1 shows the transistor has a gate, a drain, and a source, and the gate is coupled to the high power supply voltage node and the source and drain are coupled to the low power supply voltage node.

9. Claim 34 is rejected under 35 U.S.C. 103(a) as being unpatentable over Mead et al. (USP 5844265) in view of Abrokwah et al. (USP 5539248) and Manning et al. (USP 5962887).

The combination of Mead et al. and Abrokwah et al. references shows all limitations of the claim except for the transistor having gate oxide layer. However, Manning et al.'s figure 1 shows a transistor having gate oxide layer (110). Manning et al.'s transistor has the advantage of increasing voltage range. Therefore, it would have been obvious to one having ordinary skill in the art to use Manning et al.'s transistor for Mead et al. transistor for the purpose of increasing voltage range. Thus, the combination further fails to teach the gate oxide layer having thickness of between about 20 angstroms ad about 40 angstroms. However, it is seen as an obvious matter of preference bounded by well known manufacturing constraints and ascertainable by routine experimentation and optimization to choose the particular claimed relative thickness limitations because applicant has not disclosed that the limitations are for a particular unobvious purpose. produce an unexpected result, or are otherwise critical, and it appears prima facie that the process would possess utility using another relative thickness. Indeed, it has been held that optimization of range limitations are prima facie obvious absent a disclosure that the limitations are for a particular unobvious purpose, produce an unexpected result, or are otherwise critical. See MPEP 2144.05(II): "Generally, differences in concentration or temperature will not support the patentability of subject matter encompassed by the prior art unless there is evidence indicating such concentration or temperature is critical. '[W]here the general conditions of a claim are disclosed in the prior art, it is not inventive to discover the optimum or workable ranges by routine experimentation." In re Aller, 220 F.2d 454, 105 USPQ 233, 235 (CCPA 1955). See also In re Hoeschele, 406 F.2d 1403, 160 USPQ 809 (CCPA 1969), Merck & Co. Inc. v. Biocraft

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Laboratories Inc., 874 F.2d 804, 10 USPQ2d 1843 (Fed. Cir.), cert. denied, 493 U.S. 975 (1989), and In re Kulling, 897 F.2d 1147, 14 USPQ2d 1056 (Fed. Cir. 1990). As set forth in MPEP 2144.05(III), "Applicant can rebut a prima facie case of obviousness based on overlapping ranges by showing the criticality of the claimed range. 'The law is replete with cases in which the difference between the claimed invention and the prior art is some range or other variable within the claims. . . . In such a situation, the applicant must show that the particular range is critical, generally by showing that the claimed range achieves unexpected results relative to the prior art range.' In re Woodruff, 919 F.2d 1575, 16 USPQ2d 1934 (Fed. Cir. 1990). See MPEP § 716.02 - § 716.02(g) for a discussion of criticality and unexpected results." Therefore, it would have been obvious to one having ordinary skill in the art to select the thickness of Manning et al.'s layer 110 to be between 20 angstroms and about 40 angstroms dependent upon particular environment of use to ensure optimum performance.

10. Claims 35-37 are rejected under 35 U.S.C. 103(a) as being unpatentable over Choi (USP 6060930) in view of Manning et al. (USP 5962887) and McKee et al. (USP 6143072).

As to claims 35 and 36, the combination of Choi and Manning et al. references (see the rejection of claims 14 and 15) shows all limitations of the claim except for germanium die. However, McKee et al. teaches in column 1, lines 26-28, that germanium substrate is likely to provide better operating characteristics than those provided by a silicon substrate. Therefore, it would have been obvious to one having ordinary skill in the art to use germanium substrate for Choi's circuit for the purpose of improving the circuit's operating characteristics.

As to claim 37, the prior arts show all limitations of the claim except for the operational node voltage is about 1.3 volts. However, it is seen as an obvious matter of preference bounded

by well known manufacturing constraints and ascertainable by routine experimentation and optimization to choose the particular claimed relative operating voltage limitations because applicant has not disclosed that the limitations are for a particular unobvious purpose, produce an unexpected result, or are otherwise critical, and it appears prima facie that the process would possess utility using another relative operating voltage. Indeed, it has been held that optimization of range limitations are prima facie obvious absent a disclosure that the limitations are for a particular unobvious purpose, produce an unexpected result, or are otherwise critical. See MPEP 2144.05(II): "Generally, differences in concentration or temperature will not support the patentability of subject matter encompassed by the prior art unless there is evidence indicating such concentration or temperature is critical. '[W]here the general conditions of a claim are disclosed in the prior art, it is not inventive to discover the optimum or workable ranges by routine experimentation." In re Aller, 220 F.2d 454, 105 USPO 233, 235 (CCPA 1955). See also In re Hoeschele, 406 F.2d 1403, 160 USPO 809 (CCPA 1969), Merck & Co. Inc. v. Biocraft Laboratories Inc., 874 F.2d 804, 10 USPO2d 1843 (Fed. Cir.), cert. denied, 493 U.S. 975 (1989), and In re Kulling, 897 F.2d 1147, 14 USPO2d 1056 (Fed. Cir. 1990). As set forth in MPEP 2144.05(III), "Applicant can rebut a prima facie case of obviousness based on overlapping ranges by showing the criticality of the claimed range. 'The law is replete with cases in which the difference between the claimed invention and the prior art is some range or other variable within the claims. . . . In such a situation, the applicant must show that the particular range is critical, generally by showing that the claimed range achieves unexpected results relative to the prior art range.' In re Woodruff, 919 F.2d 1575, 16 USPQ2d 1934 (Fed. Cir. 1990). See MPEP § 716.02 - § 716.02(g) for a discussion of criticality and unexpected results." Therefore,

it would have been obvious to one having ordinary skill in the art to select the operating voltage for Choi's capacitor to be 1.3 volts (by selecting certain value of Vcc) dependent upon particular environment of use to ensure optimum performance.

Response to Arguments

Applicant's arguments have been fully considered, but they are not persuasive.

In response to the argument under the 102 rejections of claims 4, 14 and 15, a new ground of rejection is introduced.

In response to the arguments under the rejection Claims 9 and 10, as broad as reasonable interpretation, "a high power supply voltage node" is a node that receives a voltage that is higher other node; and "a low power supply voltage node" is a node that receives a voltage that is lower than other node. Mead et al.'s node 18 receive a voltage that is higher than node 28. Thus, node 18 is seen as a high power supply voltage node and node 28 is seen as a low supply voltage node.

In response to the arguments under 103 rejection of claims 5, 6, and 16, a new ground of rejection is introduced.

Conclusion

11. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Quan Tra whose telephone number is 703-308-6174. The examiner can normally be reached on 8:00 A.M.-5:00 P.M..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Timothy Callahan can be reached on 703-308-4876. The fax phone numbers for the

organization where this application or proceeding is assigned are 703-872-9318 for regular communications and 703-872-9319 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.

OT

September 22, 2003

Quan Tra

Patent Examiner

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